Amendments to the Specification:

Please replace the first two paragraphs of the specification with the following paragraphs:

The present application is a divisional of U.S. Patent Application Serial Number 10/055,120, filed January 21, 2002 (Docket No. 15005US03), which is a continuation of U.S. Patent Application Serial Number 09/437,721, filed November 9, 1999, which claims priority of the following provisional applications, the contents of each of which are herein incorporated by reference: Serial Number 60/107,874, entitled "Apparatus for, and Method of, Distributing Clock Signals in a Communications System," filed on November 9, 1998; Serial Number 60/108,319, entitled "Gigabit Ethernet Transceiver," filed on November 13, 1998; Serial Number 60/108,648, entitled "Clock Generation and Distribution in an Ethernet Transceiver," filed on November 16, 1998, and Serial Number 60/130,616, entitled "Multi-Pair Gigabit Ethernet Transceiver," filed on April 22, 1999.

The present invention is related to the following co-pending applications, filed on the same day as the present invention and assigned to the same assignee, the contents of each of which are herein incorporated by reference: Serial Number 09/437,724, entitled "Switching Noise reduction in a Multi-Clock Domain Transceiver," and Serial Number 09/437,719, entitled "Multi-Pair Gigabit Ethernet Transceiver."

On page 6, after the paragraph beginning "FIG. 5," please insert the following:

FIG. 5A shows another embodiment for generating the sampling clock signals.

On page 15 , please replace the second full paragraph with the following:

The 4-D output of the trellis decoder 38 is provided to the PCS receive section 204R. The receive section 204R of the PCS block de-scrambles and decodes the symbol stream, then passes the decoded packets and idle stream to the receive section ~~202T~~ 202R of the GMII block which passes them to the MAC module. The 4-D outputs, which are the error and tentative

decision, respectively, are provided to the timing recovery block 222, whose output controls the sampling time of the A/D converter 216. One of the four components of the error, and one of the four components of the tentative decision, correspond to the receiver shown in FIG. 2, and are provided to the adaptive gain stage 34 of the FFE 26 to adjust the gain of the equalizer signal path. The error component portion of the decoder output signal is also provided, as a control signal, to adaptation circuitry incorporated in each of the adaptive filters 230 and 232. Adaptation circuitry is used for the updating and training process of filter coefficients.

On page 23, please insert the following paragraph to replace the last paragraph on page 23, which continues to page 24:

It is important to note that, referring to FIG. 5, the function performed by the combination of an NCO (508, 518, 528, 538), followed by a phase selector (610, 620, 630, 640, 650, 660) can be implemented by analog circuitry. The analog circuitry can be described as follows. Each of the filtered phase errors outputted from the loop filters (506, 516, 526, 536) would be inputted to a D/A converter to be converted to analog form. Each of the analog filtered phase errors would then be inputted to a voltage-controlled oscillator (VCO). The VCOs would produce the clock signals. The VCOs can be implemented with well-known analog techniques such as those using varactor diodes. <u>This embodiment is shown in FIG. 5A.</u>